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10CS33

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. What is the difference between
(i) Analog and digital signals (ii) Ideal and Practical waveform **(04 Marks)**

b. Implement the following function using only universal gates
$\left((\overline{A}\cdot\overline{B})+\overline{C}\right) D$ **(06 Marks)**

c. Consider the black box test circuit has following logic circuit shown in Fig.Q1(c). Write verilog structural code for the given circuit. **(06 Marks)**

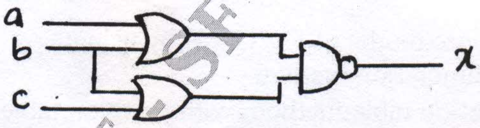

Fig.Q1(c)

d. Prove that De Morgan's two theorems with the help of truth table. **(04 Marks)**

2 a. Design logic circuit for the sum of product equation
$Y = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$
Write a general structure of Karnaugh map for four input F(A, B, C, D) **(05 Marks)**

b. With example explain entered variable. Write a truth table for entered variable map shown in Fig.Q2(b). **(05 Marks)**

	$\overline{B}$	B
$\overline{A}$	0	$\overline{C}$
A	C	1

Fig.Q2(b)

c. Simplify the following logic equation using Karnaugh map draw circuit using only NAND gates.
$F(A, B, C, D) = \sum m(7) + dc(10, 11, 12, 13, 14, 15)$ **(05 Marks)**

d. What is Hazard? With graph explain any one Hazard. **(05 Marks)**

3 a. What is multiplexer and demultiplexer? With figure explain 2 input multiplexer and 2 output demultiplexer. **(04 Marks)**

b. With figure explain 4 input exclusive – OR gate and also write truth table for four input exclusive OR gate. **(04 Marks)**

c. Explain encoder. Design an encoder which converts decimal number to BCD number. **(06 Marks)**

d. Design 7-segment decoder using programmable logic array. **(06 Marks)**

4 a. With timing diagram, describe logic circuit which generate series of negative and positive narrow pulses. **(05 Marks)**

b. With figure, explain four bit data storage by using D flip-flop. **(05 Marks)**

c. With transition diagram, explain finite state machine of all the flip-flop by using two states. **(06 Marks)**

d. Design S-R flip-flop by using D-flip-flop. **(04 Marks)**

PART – B

5 a. With neat diagram, explain serial in and serial out by using J-K flip-flop. Show how number 0100 is entered serially in a shift register using state table. **(10 Marks)**

b. Design Johnson counter by using D flip-flop. Write verilog code for a Johnson counter. **(10 Marks)**

6 a. Explain in detail mode 5 binary counter by using JK flip-flop. **(10 Marks)**

b. Explain digital clock with a block diagram. **(10 Marks)**

7 a. Reduce Moore model of Fig.Q7(a) by using
(i) Row elimination method
(ii) Implication table method, with partition table. **(10 Marks)**

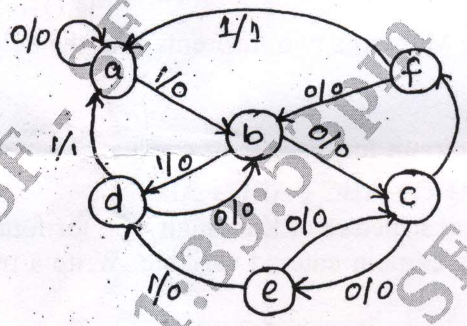

Fig.Q7(a)

b. Draw algorithm state machine for vending machine problem by Mealy model. **(10 Marks)**

8 a. With neat sketch, explain sample and hold circuit of D/A conversion. **(10 Marks)**

b. With neat diagram, explain analog to digital conversion by using simultaneous conversion method. **(10 Marks)**

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